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| **4-BIT ALU** |
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| ***DE Lab Project Report*** |
| ***Submitted By*** |
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**1. Problem Identification**

*Make a 4 Bit ALU*

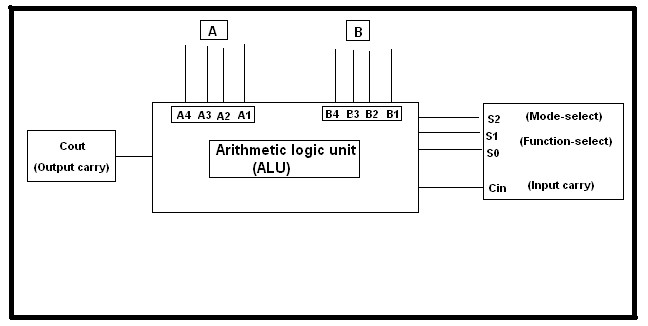
**2. Features**

It has the following functions :-



**3. Design Flow**

# Block Diagram



# Circuit Diagram

# F:\ne555\4bitALU\4bitalu.png

# Materials

1. Simulated on Proteus 8 Professional software.
2. Following materials were used in/for Proteus simulation :-

|  |  |  |
| --- | --- | --- |
| S.No | Material | Quantity |
| 1. | 7 Segment Display- Green | 3 |
| 2. | OR\_4 gate | 16 |
| 3. | Quad 2 Input (2:1) MUX | 1 |
| 4. | AND\_2 gate | 16 |
| 5. | AND\_3 gate | 40 |
| 6. | Buffer | 8 |
| 7. | Logic Probe | 5 |
| 8. | Logic State | 17 |
| 9. | NOT gate | 40 |

**4. Outcome**

# Steps of Circuit Completion

1. Made Logic for the ALU circuit.
2. Made the 4 bit ALU simulation in Proteus.

**5. Cost Analysis**

|  |  |  |
| --- | --- | --- |
| **S. No.** | **Component / Material** | **Price (in Rs.)** |
| 1. |  |  |
| 2. |  |  |
| 3. |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
| **Total** | |  |